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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,345	06/28/2001	Krishnamurthy Soumyanath	42390.P11206	8325

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/896,345	SOUMYANATH ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment received on 11/23/03 has been reviewed and considered with the following results:

As to the objection to claims 22 and 23, Applicant's amendment has overcome the objection, as such; the objection to the claims has been withdrawn.

As to the prior art rejections to the claims made in the previous Office Action mailed 6/10/03. Applicant's arguments have been fully considered but are not deemed to be persuasive. The arguments supporting the previous rejections are addressed in detail below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3, 4, 9, 10, 22, and 23 remain rejected, as per the previous Office Action, under 35 U.S.C. 102(b) as being anticipated by Kogan (US 5,321,656; previously cited).

With regard to claims 3 and 4, Kogan discloses in Fig.8C a circuit, and a method of use thereof, comprising an input port (a) having an input signal voltage; an output port (b) having an output voltage; and a field-effect-transistor (Q4) having a gate, a first terminal, and a second terminal; wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local

time-average maximum of the input signal voltage; and wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width (a typical FET has a leakage current in excess of 1 micro ampere per micron of device width; see Dai et al. US Patent No. 6,339,347); wherein the output voltage is indicative of a local time-average maximum of the input signal voltage.

With regard to claims 9 and 10, Kogan discloses in Fig.1C a circuit, and a method of use thereof, comprising an input port (a) having an input signal voltage; an output port (b) having an output voltage; and a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal; wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port; and wherein the FET (Q4) has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and wherein the output voltage is indicative of a local time-average minimum of the input signal voltage.

With regard to claim 22, the circuit further comprises an output circuit (C0, A0) connected to the output port to provide a capacitive load.

With regard to claim 23, the circuit further comprises an output circuit (C0, A0) connected to the output port to provide a capacitive load.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 12 remain rejected, as per the previous Office Action, under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Figs.1-4 in the present application, in view of Kogan.

The prior art in Figs.1-4 shows a circuit, and a method of use thereof, to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising an input port (IN in instant Fig.4) having the input signal voltage; a field-effect-transistor (402) which can be replaced by a diode (202 in Fig.2); and a DC offset correction unit (406) responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage. Figs.1-4 of the prior art meets all the claimed limitations, except for a field-effect-transistor (702 in instant Fig.7) connected as recited in the claims. Kogan teaches in Figs.8C-8D a circuit having field-effect-transistors (Q4) that is substituted for diode and is configured as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Kogan with the prior art (Figs.1-4) for the advantage of being able to reduce the size of the circuit since a diode-connected-transistor can be fabricated in CMOS technology. Furthermore, the limitation "wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width" is also met by the prior arts, note the above discussion with regard to claims 3 and 4.

Response to Arguments

6. Applicant's first argument concerning the differences between Kogan and the present invention as "All presently active claims include the claim limitations of either an output voltage

that is indicative of a local time-average maximum of the input signal voltage, or a local time-average minimum of the input signal voltage. These claim limitations are neither taught nor suggested by the cited references." is not persuasive because the output voltage of the prior art that is inherently indicative of a local time-average maximum/minimum of the input signal voltage. Even though, Kogan does not disclose that the output voltage which is indicative of a local time-average maximum/minimum of the input signal, but the output voltage still inherently being the local time-average maximum/minimum of the input signal. Since the claimed structure is fully met by the prior art of record, the resulting function claimed by applicant will be inherent, i.e., if the claimed structure is obvious, then the recited function will be inherent in the reference as modified above.

7. Applicant's second argument is that "The voltage at node b follows upward the voltage at node a, minus the threshold voltage value of transistor Q4. The voltage at node b will eventually provide the maximum of the voltage at node a (minus the threshold voltage value). However, the voltage at node b will not follow downward the voltage of node a if the voltage at node a were to decrease during the acquisition interval. This is so, because it is taught in Kogan, column 4, beginning at line 15, in regard to Figs. 1A and 2, that "when the SIGNAL and node a start to increase in voltage, node b cannot follow, but rather retains the lowest voltage that it was discharged to as it followed node a down." In understanding Fig.8C from Fig.1A, in the preceding quote from Kogan, "decrease"' is to be substituted for "increase", "highest"' for "lowest", "charged"' for "discharged", and "up" for "down" is not persuasive because the voltage at node b will inherently follow downward the voltage of node a if the voltage at node a were to decrease during the acquisition interval. Even though, Kogan ignores the leakage current that

flows through Q4 (in instant Fig.8C), but the leakage current will eventually follow downward the voltage of node a if the voltage at node a were to decrease during the acquisition interval that flows through Q4 (in instant Fig.8C), the output voltage still inherently being the local time-average maximum/minimum of the input signal. Therefore, as taught in Fig. 8C of Kogan, the voltage at node b will inherently be the local time-average maximum of the input signal voltage. Thus, the rejection to the claims is proper and remains.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178 and Right Fax number is 703-746-3951. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HLN
January 19, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800